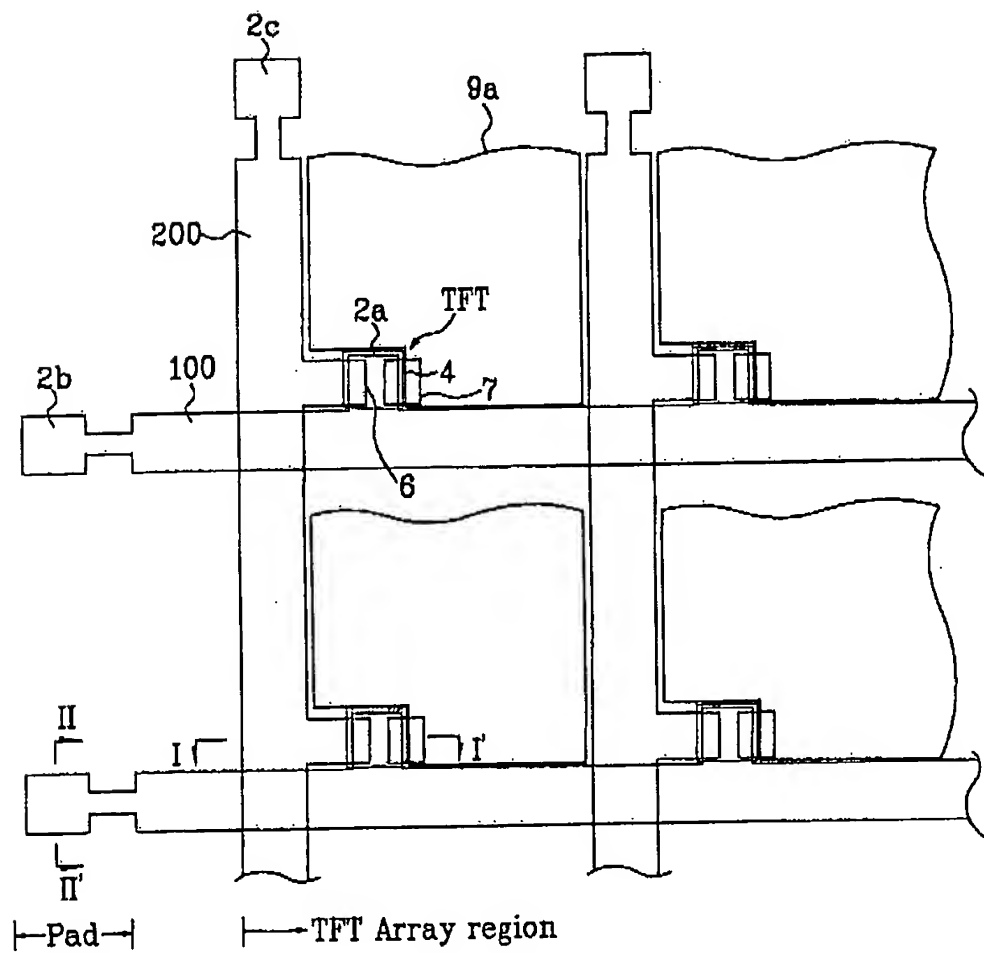


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FIG.1  
Related Art



צבר-בן ד.ח.ס. נאחיה...:

This diagram shows the cross-sectional structure of the TFT region (I) and the PAD region (II) of the semiconductor device. The TFT region (I) includes a substrate (1), a gate insulating layer (3), a gate electrode (4), a channel layer (5), a source/drain layer (6), and a passivation layer (7). The PAD region (II) includes a substrate (1), a gate insulating layer (3), a gate electrode (8), a channel layer (10), and a passivation layer (9). The regions are separated by a curved boundary line.

FIG. 3

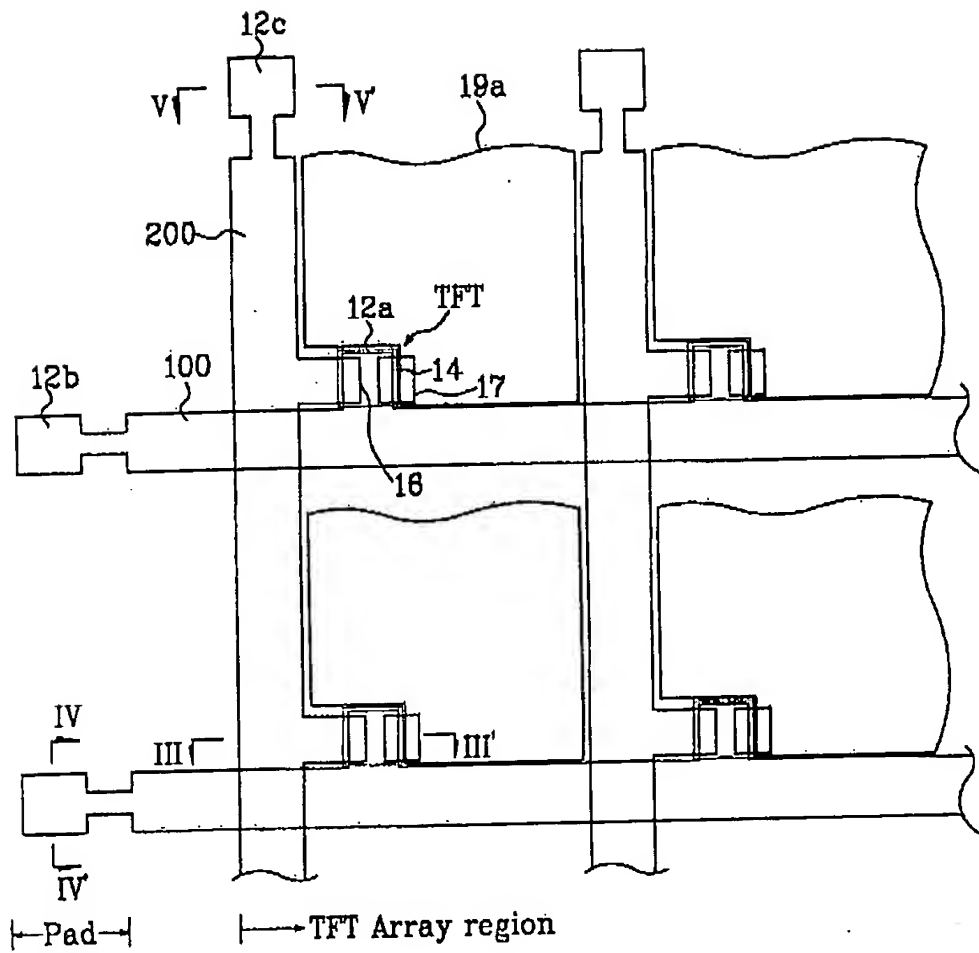


FIG. 3A

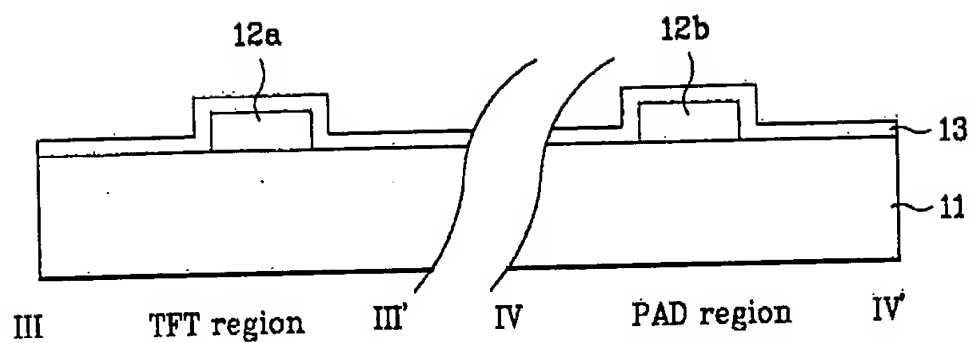
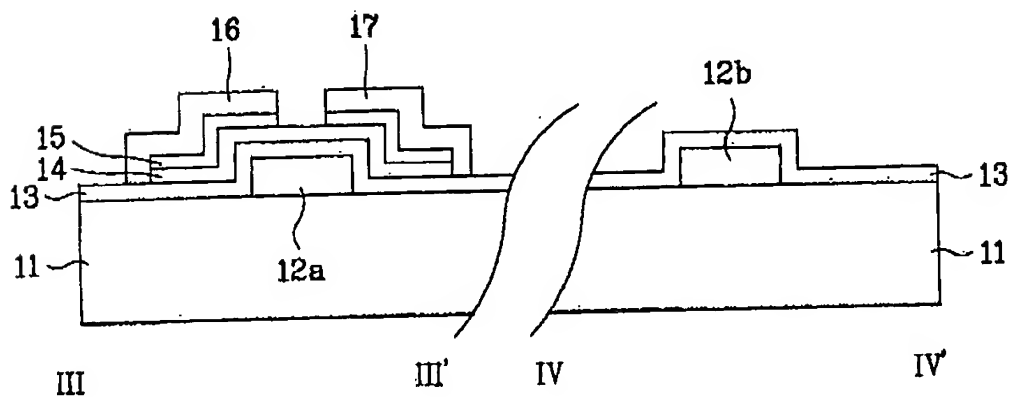
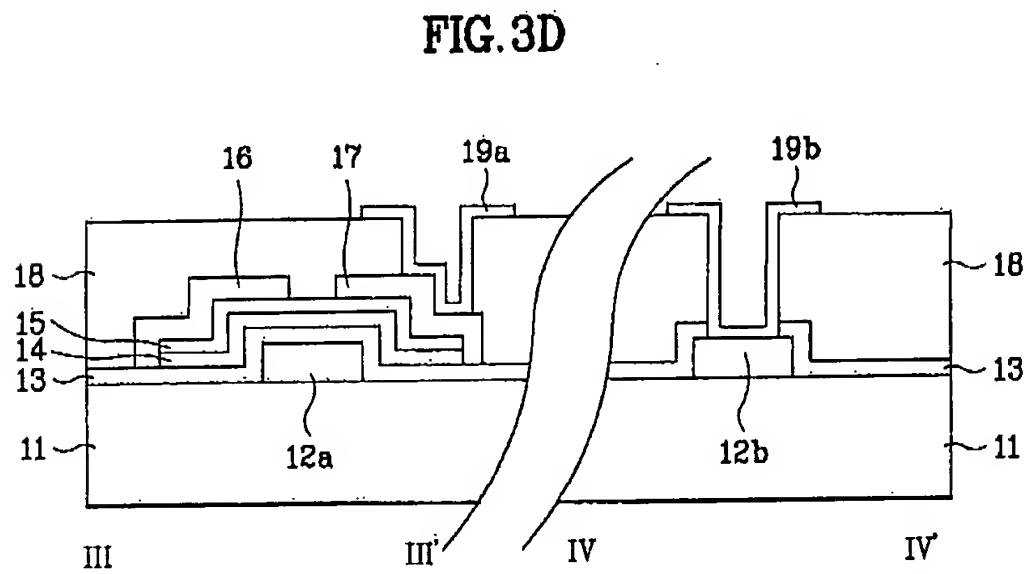
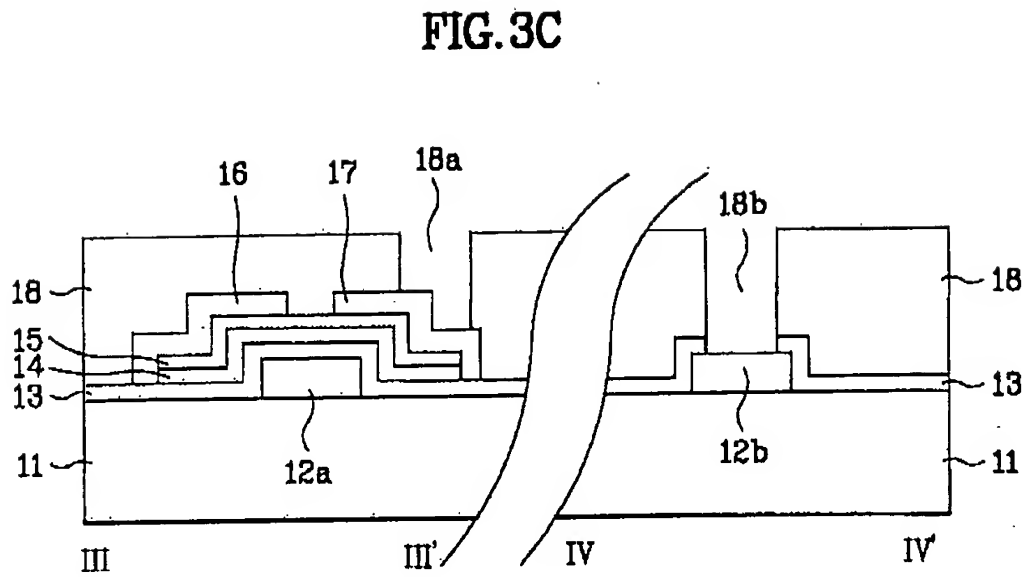


FIG. 3B





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FIG. 4A

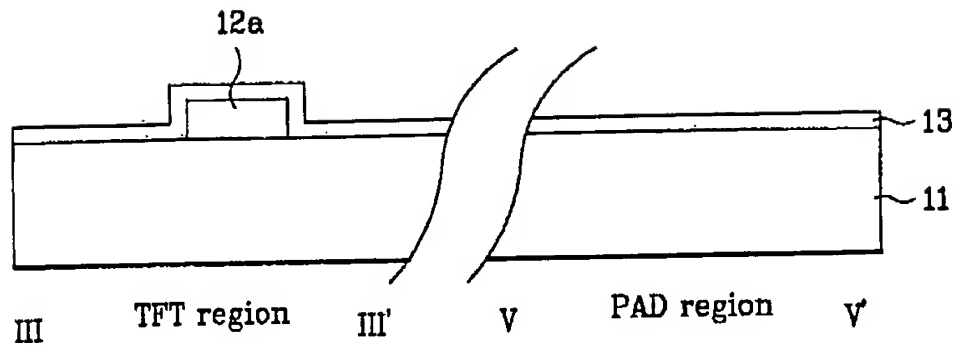


FIG. 4B

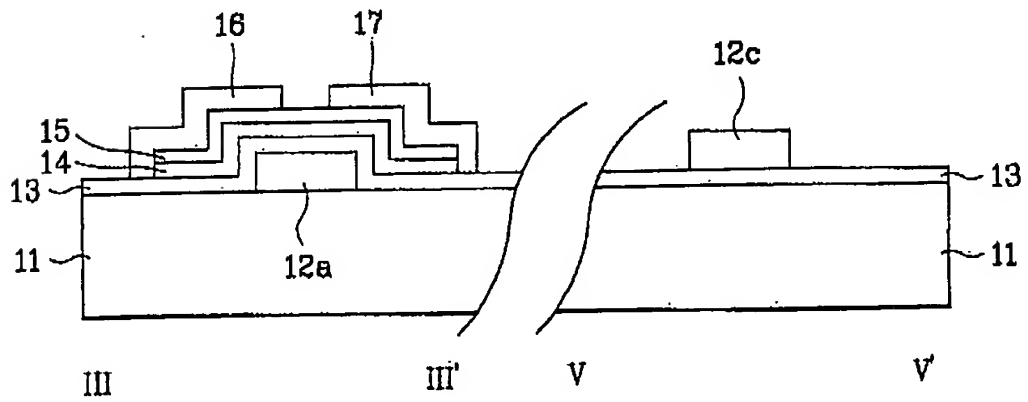


FIG. 4C

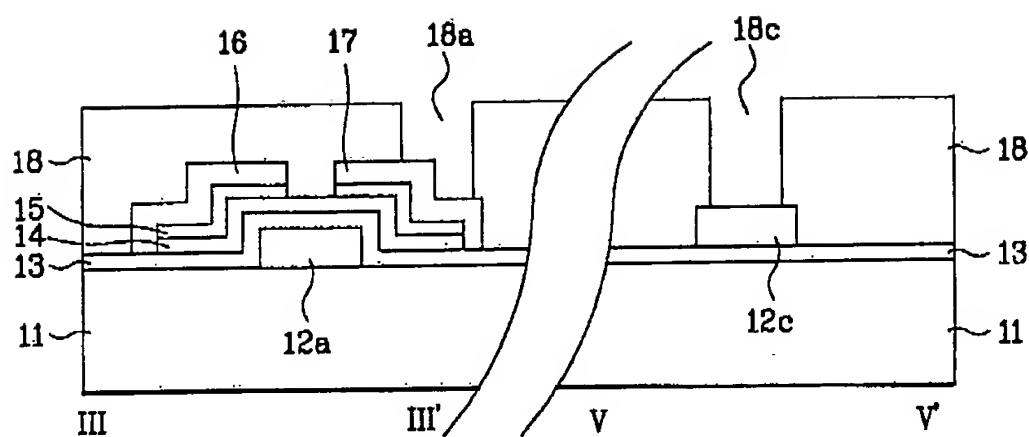


FIG. 4D

